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Effects of interface states on the transport properties of all-oxide $La_{0.8}Sr_{0.2}CoO_3/SrTi_{0.99}Nb_{0.01}O_3$ *p-n* heterojunctions

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Electrical transport properties of heteroepitaxial *p-n* junctions made of $La_{0.8}Sr_{0.2}CoO_3$ and $SrTi_{0.99}Nb_{0.01}O_3$ were studied. Junctions display highly rectifying current-voltage characteristics over a wide temperature range (20–300 K). Two distinct transport mechanisms are identified: tunneling assisted by interface states at $T<130$ K and diffusion/recombination at higher temperatures. Capacitance-voltage characteristics are used to determine the junction built-in potential at different frequencies. A capacitance relaxation is found due to charge trapping at interface states. Interface states, which deeply affect transport, are discussed in connection to charge-transfer processes related to the polarity mismatch at the interface. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2887905]

In recent years, *p-n* and Schottky junctions fabricated from transition metal oxides (TMOs) have attracted much attention.[1–4] The realization of this kind of devices is a route to change carrier concentration at the interface without the structural distortions and/or chemical disorder characteristic of doping by element substitution.[5] From the applied point of view, devices made of these materials are promising due to the fact that interface properties can be modified by external stimuli, giving rise to a wide variety of phenomena such as magnetoresistance,[6] magnetocapacitance,[7] electroresistance,[8] photocarrier control of ferromagnetism,[9] etc. In this context, the study of the electronic properties of the interface is relevant[10,11] in elucidating the mechanisms governing the aforementioned phenomena.

In this letter, we report on the fabrication and characterization of *p-n* junctions based on $La_{0.8}Sr_{0.2}CoO_3$ (LSCO) and the *n*-type semiconductor $SrTi_{0.99}Nb_{0.01}O_3$ (STNO). The parent compound $LaCoO_3$ is a charge-transfer insulator,[12] which after being doped with Sr can yield a variety of phases. Particularly in this composition range, bulk, LSCO undergoes a phase transition at ~180 K, from paramagnetic *p*-type semiconductor to a ferromagnetic metal.[13] In-plane resistivity measurements on test $x=0.20$ LSCO films on $SrTiO_3$ (STO) showed semiconductinglike behavior ($d\rho/dT<0$) in the studied temperature range (10–300 K), consistent with the observation[14] that the position of the metal to insulator transition shifts to $x>0.17$ in thin films. Transport mechanisms are explored from current-voltage[15] (*J-V*) curves and from capacitance-voltage[1] (*C-V*) measurements. We show the importance of interface states in determining the transport mechanism and the built-in potential in this system, outlining that interface states should be taken into account in modeling junctions of transition metal oxides.

Epitaxial LSCO films were deposited on both (STO) and STNO (100) substrates in a high pressure pure oxygen sputtering system at a substrate temperature of 750 °C and an oxygen pressure of 2.9 mbars. Substrates were heated in vacuum prior to sample growth. Atomic column resolution electron energy loss spectroscopy showed TiO_2 termination in all cases. After deposition samples were *in situ* annealed at 550 °C under an oxygen pressure of 900 mbars for 5 min. Evaporated Al and Ag spots (0.6 mm^2) were used as Ohmic contacts for LSCO and STNO, respectively (inset of Fig. 1). X-ray diffraction studies showed only the (100) Bragg peaks indicating *c*-axis oriented growth. Film thickness was determined to be 57 nm by x-ray reflectivity. The electrical properties of the junction were investigated by measuring current density-voltage (*J-V*), capacitance-voltage (*C-V*), and capacitance-frequency (*C-f*) characteristics at temperatures ranging from 20 to 280 K. Capacitance was measured in an HP 4284A *LCR* meter in the frequency range of 20 Hz–1 MHz.

Figure 1 shows temperature dependent *J-V* characteristics for the LSCO-STNO junction. Good rectifying behavior is found in the whole temperature range with small current values in reverse bias ($J=5\times10^{-5}$ A cm^{-2} at $V=-0.7$ V), as

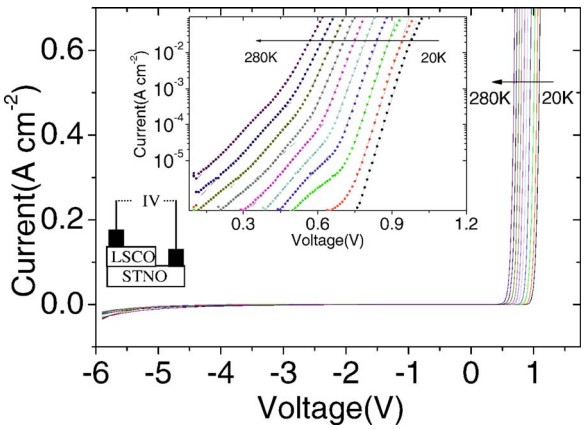

FIG. 1. (Color online) Current density-voltage characteristics of LSCO-STNO junction measured at different temperatures. Temperatures are 20, 40, 70, 100, 130, 160, 190, 220, 250, and 280 K. Insets: sketch of the heterojunction sample geometry and semilogarithmic plot of the forward bias region of the *J-V* characteristics of the main panel. Dashed lines are linear fits.

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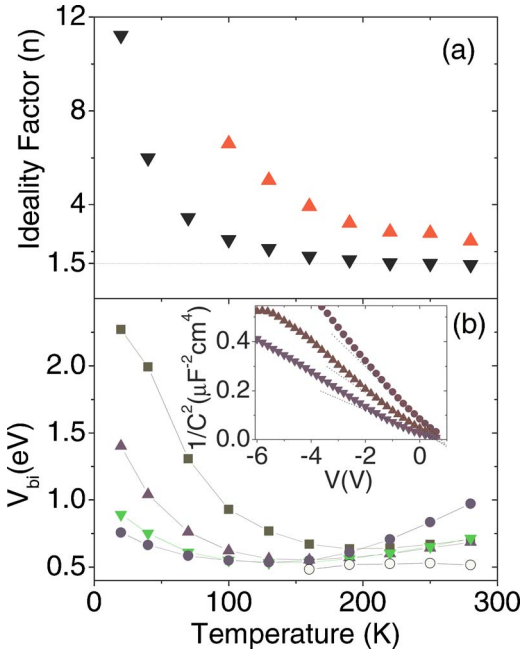

FIG. 2. (Color online) (a) Ideality factor of a LSCO-STNO *p-n* junction as function of temperature. (b) Temperature dependence of the built-in potential barrier of a LSCO-STNO *p-n* junction calculated from capacitance-voltage measurements made at different frequencies: 100 Hz (circle), 1 kHz (downward triangle), 10 kHz (upward triangle), and 100 kHz (square). Open circles: built-in potential barrier calculated from *J-V* measurements. Inset: typical $1/C^2$-*V* measurements at 1 kHz. Dashed lines are linear fits for the low reverse bias region (between −1 and 0 V).

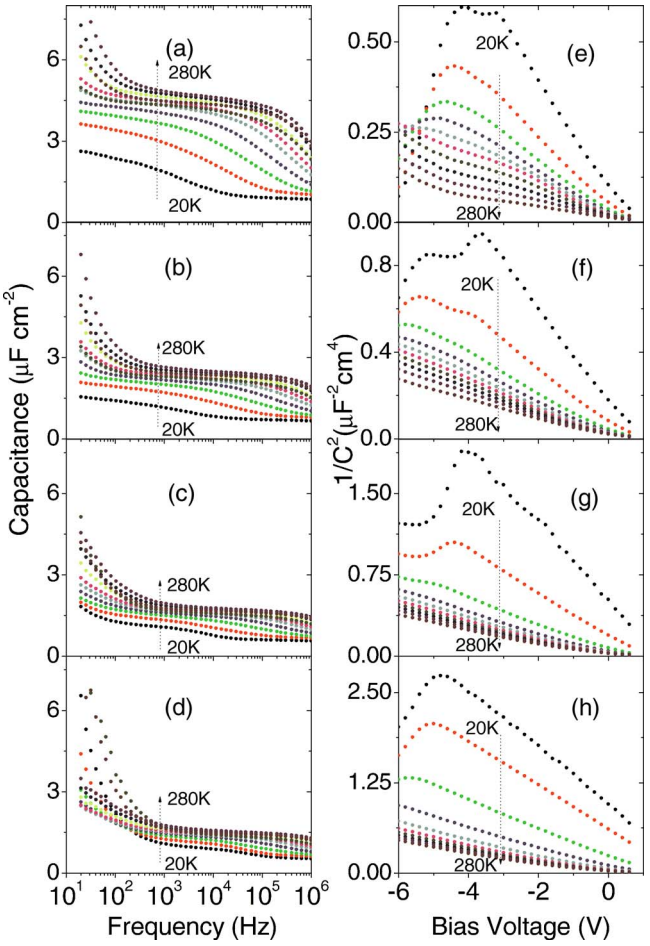

FIG. 3. (Color online) [(a)–(d)] Temperature dependent capacitance-frequency characteristics of a LSCO-STNO *p-n* junction at reverse bias voltage, from top to bottom: −0.5, −2.5, −4.5, and −5.5 V. [(e)–(h)] Temperature dependent capacitance-voltage characteristics of a LSCO-STNO *p-n* at different frequencies, from top to bottom: 100 Hz, 1 kHz, 10 kHz, and 100 kHz. Temperature values are the same as in Fig. 1.

compared to forward bias (J=0.7 A cm^{-2} at V=0.7 V). In the abrupt *p-n* junction model, when $V > k_BT/q$, we can approximate the forward bias current density (J_F) as[16]

$$J_F = J'_{pn} \exp\left(\frac{qV}{nk_BT}\right), \tag{1}$$

$$J'_{pn} \propto T \exp\left(-\frac{qV_{bi}}{k_BT}\right), \tag{2}$$

where V_{bi} is the built-in potential, q is the elementary charge, k_B is the Boltzmann constant, T is the junction temperature, V is the bias applied, and n is the ideality factor. In the ideal diffusion mechanism n equals to 1, whereas n equals to 2 when current transport is dominated by recombination of charge carriers in the space charge region.[16] Current density is in fact exponential with the forward bias voltage (see inset of Fig. 1), although for temperatures between 300 and 100 K, there are two distinct regions at low and high biases with different slopes. Figure 2(a) displays the ideality factor n obtained from the slopes of the *J-V* curves. The value $n \sim 1.5$ obtained in the high bias region at room temperature is similar to that obtained by other authors for other TMO high quality junctions.[10] On the other hand, we obtain $n \sim 2.7$ in the low bias region at high temperatures. This is the signature of two different mechanisms for current transport, one in the low bias region dominated by recombination of carriers and other in the high bias region dominated by diffusion. At low temperatures, below 130 K, the ideality factor reaches unphysical values, which implies that Eq. (1) is no longer applicable. In this temperature range (20–100 K) the slope of the log J versus V plot no longer varies as $1/T$, actually, it is almost temperature independent. This result points to charge carrier tunneling in the junction, most likely assisted by interface states. This mechanism has been previously observed in a manganite-titanate *p-n* and Schottky junctions.[4,17] We estimated V_{bi} values from the temperature dependence of J'_{pn} [Eqs. (1) and (2)] according to which $\ln J'_{pn}/T$ is proportional to qV_{bi}/k_BT. V_{bi} (open circles, Fig. 2) was obtained from the temperature dependence of J'_{pn} between 190 and 290 K.

Next, we describe the capacitance (*C-V* and *C-f*) characterization of the junctions. The depletion capacitance is defined as $C = dQ/dV$, where dQ is the incremental change in the depletion layer charge for an incremental change in the applied voltage dV. This is the only significant contribution to the capacitance under reverse bias. In the abrupt junction model, the voltage dependence of $1/C^2$ can be expressed as[16]

$$\frac{1}{C^2} = \frac{2}{q}\left(\frac{1}{\varepsilon_{STNO}N_{STNO}} + \frac{1}{\varepsilon_{LSCO}N_{LSCO}}\right)(V_{bi} - V), \tag{3}$$

where ε_{STNO} and ε_{LSCO} are the permittivities of STNO and LSCO, respectively, N_{STNO} and N_{LSCO} are the carrier densities, and V_{bi} is the built-in potential across the heterojunction interface.

Figures 3(a)–3(d) depict capacitance-frequency measurements at reverse bias voltage of −0.5, −2.5, −4.5, and −5.5 V. A capacitance relaxation is observed at a tempera-

ture dependent (but essentially bias independent) frequency. Capacitance relaxations at high frequencies are typically due to charge trapping/detrapping processes at interface states or deep levels. It may also arise from electric field relaxation which occurs at frequencies $f_r \sim 1/2\pi R_s C$, where R_s is the series resistance associated with the junction. We estimate this frequency to be $f_r \sim 10^7$ Hz at 20 K and even larger at higher temperatures. Since this value is more than four orders of magnitude larger than the relaxation frequency observed at this temperature, we can exclude this mechanism as being responsible for capacitance relaxation. The bias independence of the characteristic frequency also excludes deep levels within the space charge region and points to charge trapped at (electronlike) interface states in equilibrium with the electron quasi-Fermi level on the STNO side. On the other hand, the low frequency dispersion of the capacitance below 300 Hz for different temperatures depends on the bias voltage and is most likely due to hole (like) deep levels at the LSCO side. *C-V* plots will be thus influenced by relaxation phenomena and the use of Eq. (3) may produce unrealistic values of the built-in potential. It is thus important to determine the region in which Eq. (3) remains valid.

Figures 3(e)–3(h) show *C-V* characteristics at four different frequencies: 100 Hz, 1 kHz, 10 kHz, and 100 kHz. A linear dependence of $1/C^2$ on V is observed at low values of the reverse bias voltage. We have used linear fits to Eq. (3) between −1 and 0 V to obtain (from the intercepts with the voltage axis) the built-in potential V_{bi} for each temperature and frequency. The obtained V_{bi} values are presented in Fig. 2(b). The unphysical high values below 100 K at frequencies greater that 100 Hz result from the relaxation of the capacitance. Notice, however, that for temperatures above 200 K, V_{bi} values obtained with different measurement frequencies (1, 10, and 100 kHz) coincide, providing a measure of V_{bi}, which should be in fact independent of frequency. The value obtained from the 100 Hz measurement is abnormally high as a consequence of the low frequency dispersion of the capacitance [see Fig. 3(a)–3(d)].

From the above experimental results, it is clear that it is not possible to obtain the built-in potential using $1/C^2$-V characteristics using a single frequency measurement over the whole temperature range. Instead, different frequencies should be used to ascertain the relative influence of the different contributions to the capacitance on the V_{bi} determination. Within the appropriate frequency range [see Fig. 2(b)], different frequencies provide the same consistent value of the built in potential, $V_{bi}=0.6\pm0.1$ V, almost temperature independent.

Both current voltage and capacitance characterization agree in showing the presence of interface states. We argue that the states assisting the tunneling process at low temperatures (*J-V*) are the same which trap charge and cause the capacitance relaxation (*C-f-V*). Notice that the unrealistically large values of the built-in potential (denouncing interface charge relaxation) occur in the same temperature range where the tunneling assisted transport is observed. The origin of interface states may be related to the electronic reconstruction resulting from charge leakeage[18] or to the disruption in the charge sequence (polarity mismatch) at the interface, which dopes the interface TiO_2 plane with electrons.[19] Charge trapped at interface states may be thus essential in determining band discontinuities and the built-in potential.

In summary, we studied the transport mechanisms of heteroepitaxial LSCO-STNO *p-n* junction. We established that in the range of temperatures from 100 to 300 K recombination current dominates at low bias voltage, while diffusion current dominates at high bias voltage. Below 100 K, transport is dominated by interface state-assisted electron tunneling. Charge trapped at interface states also determines the built-in potential and is responsible for capacitance relaxation phenomena. These results underline the importance of interface states in determining junction properties and future modeling of junctions of transition metal oxides should consider their contribution.

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